RAM BANK B

RAM BANK A

Decoupling capacitors place close to U4

Peripheral Control
Data Bus
Address Bus
Misc. Bus

SET ROM HIGH
SET ROM TO 8-BIT
UNUSED (MIN/MAX)
UNUSED (NOCPU)
SET CPU TO 16-BIT
SET BIG-ENDIAN
UNUSED (EXTCLK)
SET CPU TO 68K BUS
SET DRAM TO TWO-CAS

OBERON CONFIGURATION BITS

DSP PRIVATE MEMORY INTERFACE
Socket here with 256K x 4 DRAM, may also be fitted with 1M x 4 DRAM, or two DRAMs or up to 1 MB ROM (requires 1 TTL device also)

EXPANSION CONNECTOR

MINI EXPANSION PORT

LINK
SHEET2.SCH
SHEET3.SCH
SHEET4.SCH
SHEET5.SCH